



## ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18  
 Stylesheet Version v18.0

Title of Invention	Integrated circuit wiring architectures to support independent designs											
Application Number:	09/739582 											
Confirmation Number:	3530											
First Named Applicant:	Steven Teig											
Attorney Docket Number:	SPLX.P0005											
Art Unit:	2815											
Examiner:	Chris C. Chu											
Search string:	( 5637920 or 5640327 or 5646830 or 5650653 or 5689433 or 5784289 or 5801385 or 5822214 or 5880969 or 5889329 or 6111756 or 6150193 or 6260183 or 6301686 or 6307256 or 6316838 or 6324674 or 6412097 or 6516455 or 6645842 or 20010009031 or 20020069397 or 20030025205 ).pn.											
<b>US Patent Documents</b>												
Note: Applicant is not required to submit a paper copy of cited US Patent Documents												
init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass					
C.C.	1	5637920	1997-06-10	Loo	A	257	700					
C.C.	2	5640327	1997-06-17	Ting	A	716	7					
C.C.	3	5646830	1997-07-08	Nagano	A	361	813					
C.C.	4	5650653	1997-07-22	Rostoker et al.	A	257	369					
C.C.	5	5689433	1997-11-18	Edwards	A	716	2					
C.C.	6	5784289	1998-07-21	Wang	A	716	8					
C.C.	7	5801385	1998-09-01	Endo et al.	A	250	370.11					
C.C.	8	5822214	1998-10-13	Rostoker et al.	A	716	10					
C.C.	9	5880969	1999-03-09	Hama et al.	A	716	12					
C.C.	10	5889329	1999-03-30	Rostoker et al.	A	257	758					
C.C.	11	6111756	2000-08-29	Moresco	A	361	735					
C.C.	12	6150193	2000-11-21	Glenn	A	438	113					
C.C.	13	6260183	2001-07-10	Raspopovic et al.	B1	716	12					

C.C.	14	6301686	2001-10-09	Kikuchi et al.	B1	716	2
C.C.	15	6307256	2001-10-23	Chiang et al.	B1	257	668
C.C.	16	6316838	2001-11-13	Ozawa et al.	B1	257	778
C.C.	17	6324674	2001-11-27	Andreev et al.	B2	716	12
C.C.	18	6412097	2002-06-25	Kikuchi et al.	B1	716	2
C.C.	19	6516455	2003-02-04	Teig et al.	B1	716	7
C.C.	20	6645842	2003-11-11	Igarashi et al.	B2	438	598

## US Published Applications

Note: Applicant is not required to submit a paper copy of cited US Published Applications

init	Cite.No.	Pub. No.	Date	Applicant	Kind	Class	Subclass
C.C.	1	20010009031	2001-07-19	Nitta et al.	A1	716	13
C.C.	2	20020069397	2002-06-06	Teig et al.	A1	716	12
C.C.	3	20030025205	2003-02-06	Shively	A1	257	758

Signature

Examiner Name	Date
<i>Christie</i>	11/12/04



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Substitute for form 1449A/PTO <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> <i>(use as many sheets as necessary)</i>				Application Number	09/739,582
				Filing Date	12/15/2000
				First Named Inventor	Steven Teig
				Group Art Unit	2815
				Examiner Name	Chris Chu
Sheet	1	of	2	Attorney Docket Number	SPLX.P0005

FOREIGN PATENT DOCUMENTS						
Examiner* Initials	Cite No. <sup>1</sup>	Foreign Patent Document		Date of Publication	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Office <sup>3</sup>	Number <sup>4</sup>	Kind Code (If Known) <sup>5</sup>		T <sup>6</sup>
C.C.	1.	JP	2000-082743		03-21-2000 Igarashi et al.	with Japanese Patent Office's English translation of Abstract; and with English translation of the application. ✓

NON PATENT LITERATURE DOCUMENTS						
Examiner* Initials	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.				
C.C.	2.	Chen et al., Optimal Algorithms for Bubble Sort Based Non-Manhattan Channel Routing, May 1994, Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions Volume: 13 Issues, pp. 603-609.				
C.C.	3.	Chen, H. et al., Physical Planning of On-Chip Interconnect Architectures, 2002, IEEE, International Conference, pp. 30-35				
C.C.	4.	Cong J. et al., DUNE – A Multilayer Gridless Routing System, May 2001, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol 20, iss. 5, pp. 633-647.				
C.C.	5.	Dion J. et al., Contour: A Tile-based Gridless Router, March 1995, Digital Western Research Laboratory, research Report 95/3, pp.1-22				
C.C.	6.	Merriam-Webster's Collegiate Dictionary, 10 <sup>th</sup> edition, Merriam-Webster Incorporated, p.606				
C.C.	7.	Morton, P. B. et al., An Efficient Sequential Quadratic Programming Formulation of Optimal Wire Spacing for Cross-Talk Noise Avoidance Routing, UCSC-CRL-99-05, March 10, 1999.				
C.C.	8.	NN71091316, Use of Relatively Diagonal And Rectangular Wiring Planes n Multilayer Packages, September 1971, IBM Technical Disclosure Bulletin, Vol. No. 14, Issue No. 4, pp. 1316-1317.				

Examiner Signature	<i>Chris Chu</i>	Date Considered	11/12/04
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\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. <sup>1</sup> Applicant's unique citation designation number(optional). <sup>2</sup> See Kinds Codes of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04. <sup>3</sup> Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>5</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. <sup>6</sup> Applicant is to place a check mark here if English language Translation is attached.

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**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

Sheet	2	of	2	Application Number	09/739,582
				Filing Date	12/15/2000
				First Named Inventor	Steven Teig
				Group Art Unit	2815
				Examiner Name	Chris Chu
				Attorney Docket Number	SPLX.P0005

**NON PATENT LITERATURE DOCUMENTS**

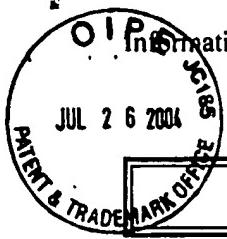
Examiner Initials	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>6</sup>
C.C	9.	Royle, J. et al., Geometric Compaction in One Dimension for Channel Routing, 24 <sup>th</sup> ACM/IEEE Design Automation Conference, 1987, pp 140-145.	
C.C	10.	Schiele, W. et al., A Gridless Router for Industrial Design Rule, 27 <sup>th</sup> ACM-IEEE Design Automation Conference, pp. 626-631, 1990.	
C.C	11.	Tseng H. et al., A Gridless Multilayer Router for Standard Cell Circuits Using CTM Cells, Oct. 1999, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol 18, iss. 10, pp. 1462-1479.	

Examiner Signature		Date Considered	11/12/04
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Examiner Name	Date
<i>Christina</i>	11/12/04